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Lou 13-13

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Hui-Ling Lou et al.

Case: 13-13

Serial No.: 09/390,389

Filing Date: September 3, 1999

Group: 2631

Examiner: Kevin Michael Burd

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class, mail addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Signature: *V. Benclun* Date: May 11, 2004

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Title: Multiplier-Free Methods and Apparatus for Signal Processing in a Digital Communication System

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby appeal the final rejection dated December 8, 2003 of claims 1-5, 10-16, 21, 22 and 24 of the above-identified application.

REAL PARTY IN INTEREST

The present application is assigned to Agere Systems Inc. The assignee Agere Systems Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals and interferences.

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STATUS OF CLAIMS

The present application was filed on September 3, 1999 with claims 1-25. Claims 6, 7, 17, 18, 23 and 25 were canceled in an amendment filed on March 7, 2003. Claims 1-5, 8-16, 19-22 and 24 are currently pending in the present application. Claims 1, 12 and 24 are the independent claims.

Claims 1-5, 10-16, 21, 22 and 24 stand rejected under 35 U.S.C. §103(a). Claims 8, 9, 19 and 20 are indicated as containing allowable subject matter. Claims 1-5, 10-16, 21, 22 and 24 are appealed.

STATUS OF AMENDMENTS

There have been no amendments filed subsequent to the final rejection.

SUMMARY OF INVENTION

The present invention is directed to arrangements for processing information in a receiver of a digital communication system. A signal processing operation is applied to a sequence of transmitted symbols, where each of the symbols represents a particular number of information bits and corresponds to a point in a first modulation constellation. The first modulation constellation corresponds to a rotated version of a second modulation constellation. The signal processing operation utilizes at least one selector to compute a product of a channel estimate and a given one of the transmitted symbols. More specifically, the selector receives as inputs real and imaginary parts of an element of the channel estimate, and generates as outputs real and imaginary parts of a product of the element of the channel estimate and a corresponding element of the given symbol, without requiring a multiplication operation.

Illustrative embodiments of the invention are described in the specification at, for example, page 7, line 20, to page 10, line 25, and are shown in the computational structures in FIGS. 3-6, 8, 9, 11, 13, 14 and 16 of the drawings.

The claimed arrangements provide important advantages over conventional techniques. For example, as indicated in the specification at page 3, lines 9-14, and page 4, lines 1-9, the invention in an illustrative embodiment can eliminate or substantially reduce the number of required

multipliers, and thus “significantly reduces the complexity and delay associated with the corresponding signal processing circuitry.”

ISSUE PRESENTED FOR REVIEW

Whether claims 1-5, 10-16, 21, 22 and 24 are unpatentable under 35 U.S.C. §103(a) over U.S. Patent No. 6,233,271 (hereinafter “Jones”) in view of pages 266-269 of a textbook by R.H. Katz entitled “Contemporary Logic Design” (hereinafter “Katz”).

GROUPING OF CLAIMS

With regard to the above-identified issue, claims 1-5, 12-16 and 24 stand or fall together, claims 10 and 21 stand or fall together, and claims 11 and 22 stand or fall together.

ARGUMENT

A proper *prima facie* case of obviousness requires that the cited references when combined must “teach or suggest all the claim limitations,” and that there be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references or to modify the reference teachings. See Manual of Patent Examining Procedure (MPEP), Eighth Edition, August 2001, §706.02(j).

Applicants submit that the Examiner has failed to establish a proper *prima facie* case of obviousness in the present §103(a) rejection, in that the Jones and Katz references, even if assumed to be combinable, fail to teach or suggest all the claim limitations, and in that no cogent motivation has been identified for combining the references or modifying the reference teachings to reach the claimed invention. Further, even if it is assumed that a proper *prima facie* case has been established, there are particular teachings in one or more of the references which controvert the obviousness argument put forth by the Examiner.

Independent claim 1 is directed to a method of processing information in a receiver of a digital communication system. The claim includes, among other limitations, the following limitations denoted (a) and (b) herein for ease of discussion:

(a) a signal processing operation applied to a sequence of transmitted symbols utilizes at least one selector to compute a product of a channel estimate and a given one of the transmitted symbols; and

(b) the selector receives as inputs real and imaginary parts of an element of the channel estimate, and generates as outputs real and imaginary parts of a product of the element of the channel estimate and a corresponding element of the given symbol, without requiring a multiplication operation.

As indicated previously herein, illustrative examples of arrangements falling within limitations (a) and (b) of claim 1 are described in the specification at, for example, page 7, line 20, to page 10, line 25, and shown in the computational structures in FIGS. 3-6, 8, 9, 11, 13, 14 and 16 of the drawings.

The Examiner in formulating the §103(a) rejection argues that limitations (a) and (b) are found in the combined teachings of Jones and Katz. In support of his position, the Examiner relies on the teachings in FIG. 16, column 12, lines 30-48, and the abstract of Jones, and the teachings in FIG. 5.28 and page 267 of Katz. The cited text from Jones, relied upon by the Examiner, provides as follows:

A method and an apparatus for decoding trellis coded direct sequence spread spectrum communication signals are provided. A transmitted QPSK signal is received. Binary phase-shift keyed (BPSK) despreading is performed on the QPSK signal. The BPSK despreading comprises correlating the in-phase and the quadrature components of the received QPSK signal with independent PN sequences for the each of the in-phase and the quadrature components. The despread signal is then demultiplexed, and the pilot signal and the BPSK data signal are recovered. The recovered pilot signal is used to provide a channel phase estimate and a channel magnitude estimate. The recovered BPSK data signal is demodulated, despread, and decoded. The despreading and decoding comprises determining a number of cross-correlation terms of the received signal using a number of transmitted biorthogonal Walsh sequences. The cross-correlation terms are used as the branch metrics

in a maximum likelihood decoding algorithm. The branch metrics may be computed with a Fast Walsh Transform scaled in response to the channel phase estimate from the recovered pilot signal. The maximum likelihood decoding algorithm may be a Viterbi algorithm in which the optimum path is the path with the maximum accumulated branch metric. The decoding algorithm recovers and outputs a transmitted data bit sequence.

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FIG. 16 is the channel estimation and maximal ratio combining in the receiver of one embodiment. . . . The pilot in this case is overlaid with the Walsh (0) sequence 1814. The pilot signal 1804, attained using the W(0) sequence 1814, is used to as a channel estimate of the phase and magnitude of the received signal. This channel estimate is used to rotate and scale, based on current channel conditions, the other Walsh components 1816 of the FHT prior to being sent to the decoder. The rotating and scaling is performed by delaying each component of the FHT in order to center the data with the phase estimate interval. The delayed components are then each multiplied 1818 by the complex conjugate 1806 of the pilot signal. The real part 1808 and 1810 of each component is sent to the decoder 1812 when soft decisions are required; otherwise the maximum component of the phase-compensated FHT is found given the hard decision.

Applicants have carefully reviewed the above-cited passages from Jones, as relied on by the Examiner, as well as FIG. 16, and are unable to find any teaching whatsoever regarding limitations (a) and (b). More specifically, the relied-upon portions of Jones fail to make any mention regarding a signal processing operation which utilizes at least one selector to compute a product of a channel estimate and a given one of the transmitted symbols, as set forth in limitation (a). In fact, a keyword search conducted by the undersigned in an electronic version of the Jones reference taken from the USPTO patent database indicates that the term “selector” does not appear anywhere in the text of the Jones reference. Since Jones fails to make mention of any selector whatsoever, it is clear that Jones cannot be relied upon for teaching a selector having the particular configuration recited in limitation (b), namely, a selector which receives as inputs real and imaginary parts of an element of

the channel estimate, and generates as outputs real and imaginary parts of a product of the element of the channel estimate and a corresponding element of the given symbol.

The Katz reference fails to supplement the fundamental deficiencies of Jones as applied to limitations (a) and (b). FIG. 5.28 of Katz shows a 4x4 combinational adder circuit, which at best may be characterized as a multiplier which is implemented using adders. The collective teachings of Katz and Jones fail to make any mention whatsoever regarding the claimed selector and its configuration.

Claim 1 thus includes one or more limitations which are not taught or suggested by the proposed combination of Jones and Katz. The combined teachings of these references therefore fail to “teach or suggest all the claim limitations” as would be required by a proper §103(a) rejection.

Also, as indicated previously, the Examiner has failed to identify a cogent motivation for combining the references or for modifying the reference teachings to reach the claimed invention.

Applicants initially submit that Jones and Katz are in fact non-analogous art relative to one another. Jones is in the communication system art and relates to decoding trellis coded direct sequence spread spectrum communication signals. Katz is in the digital logic design art and deals with logic design for arithmetic circuitry such as adders. One looking to improve signal processing operations for spread spectrum communication signals as in Jones would not be motivated, absent some explicit suggestion, to look toward the digital logic design art for teachings regarding digital adders. This disparity in the technical fields of Jones and Katz is indicative of a lack of motivation to combine the references.

As was described above, neither Jones nor Katz teaches or suggests the particular limitations (a) and (b) of claim 1. However, the Examiner argues that it would be obvious to combine or modify the teachings of these references to meet the limitations in question because “[t]he logic and adders will eliminate computational complexity of the multipliers of Jones and simpler components can be used in their stead” (Final Office Action, page 4, last paragraph). Applicants submit that this is a conclusory statement of obviousness, and insufficient to support the proposed combination or modification of the reference teachings.

The Federal Circuit has stated that when patentability turns on the question of obviousness, the obviousness determination “must be based on objective evidence of record” and that “this

precedent has been reinforced in myriad decisions, and cannot be dispensed with.” In re Sang-Su Lee, 277 F.3d 1338, 1343 (Fed. Cir. 2002). Moreover, the Federal Circuit has stated that “conclusory statements” by an examiner fail to adequately address the factual question of motivation, which is material to patentability and cannot be resolved “on subjective belief and unknown authority.” Id. at 1343-1344. There has been no showing in the present § 103(a) rejection of objective evidence of record that would motivate one skilled in the art to combine Jones and Katz or to modify the proposed combination of Jones and Katz to produce the particular limitations in question. The above-quoted statement of obviousness given by the Examiner in the Office Action is precisely the type of subjective, conclusory statement that the Federal Circuit has indicated provides insufficient support for an obviousness rejection. It appears, in view of the above-quoted conclusory statement of obviousness provided by the Examiner, that the Examiner in combining Jones and Katz has simply undertaken a hindsight-based piecemeal reconstruction of the claimed invention based on the disclosure provided by Applicants. Such an approach is improper.

Further, even if it is assumed that a proper *prima facie* case has been established, there are particular teachings in one or more of the references which controvert the obviousness argument put forth by the Examiner. For example, the Jones reference, as characterized by the Examiner, utilizes multiplication operations in the portion thereof which is alleged to disclose the claimed selector. This is a direct teaching away from the claimed invention, which calls for a selector that performs a particular function without requiring a multiplication operation. Such a teaching away constitutes evidence of non-obviousness.

Applicants therefore respectfully submit that independent claim 1 is allowable over Jones, Katz and the other art of record. The § 103(a) rejection is believed to be improper, and should be withdrawn.

Independent claims 12 and 24 include limitations similar to those of claim 1, and are therefore believed to be allowable for substantially the same reasons identified above with regard to claim 1.

Dependent claims 2-5, 10-11, 13-16, 21 and 22 are believed allowable for at least the reasons identified above with regard to their respective independent claims. Moreover, these claims are

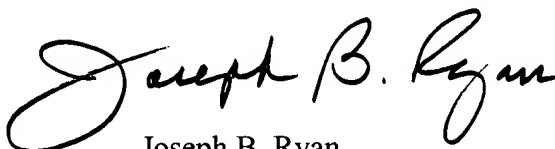
believed to define additional separately-patentable subject matter relative to the proposed combination of Jones and Katz.

With regard to dependent claims 10 and 21, each of these claims generally specifies that the signal processing operation comprises a multi-stage multiplication operation implemented without multiplication operations, wherein each stage of the multi-stage operation corresponds to a selector, and a left shift element is arranged between an output of a given one of the stages and a corresponding input of a subsequent stage. The Examiner argues that dependent claims 10 and 21 are obvious because “Katz discloses how the input signal is processed before being input to the decoder of Jones” (Final Office Action, page 5, fourth paragraph). This conclusory statement is believed to be an incorrect characterization of the teachings of the Jones and Katz references. The Examiner further argues in an Advisory Action dated March 25, 2004, that the limitations in question are met by the 4x4 combinational adder circuit shown in FIG. 5.28 of Katz. However, as indicated above, this relied-upon adder circuit of Katz fails to provide the selector functionality called for in the claims.

With regard to dependent claims 11 and 22, these claims call for implementation of a selector-based signal processing operation and a selector-based signal processing circuit, respectively, utilizing a multi-stage hierarchical adder tree without multiplication operations. The Examiner in the final Office Action fails to identify with specificity the particular portions of the cited references which are alleged to meet the particular limitations set forth in claims 11 and 22. There is no teaching or suggestion in the cited art, taken individually or in combination, regarding the selector-based limitations set forth in claims 11 and 22.

In view of the above, Applicants believe that claims 1-5, 8-16, 19-22 and 24 are in condition for allowance, and respectfully request withdrawal of the §103(a) rejection.

Respectfully submitted,

A handwritten signature in black ink that reads "Joseph B. Ryan". The signature is fluid and cursive, with the first name "Joseph" being more prominent than the last name "Ryan".

Date: May 11, 2004

Joseph B. Ryan
Attorney for Applicant(s)
Reg. No. 37,922
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-7517

APPENDIX

1. (Amended) A method of processing information in a receiver of a digital communication system, the method comprising the step of:

applying a signal processing operation to a sequence of transmitted symbols, wherein the transmitted symbols correspond to points in a first modulation constellation, the first modulation constellation corresponds to a rotated version of a second modulation constellation, and each of the transmitted symbols represents a particular number of information bits;

the signal processing operation utilizing at least one selector to compute a product of a channel estimate and a given one of the transmitted symbols;

wherein the selector receives as inputs real and imaginary parts of an element of the channel estimate, and generates as outputs real and imaginary parts of a product of the element of the channel estimate and a corresponding element of the given symbol, without requiring a multiplication operation.

2. (Original) The method of claim 1 wherein use of the first modulation constellation allows the signal processing operation to be performed without multiplication operations.

3. (Original) The method of claim 1 wherein the first modulation constellation is generated by applying a 45° rotation to the second modulation constellation.

4. (Original) The method of claim 1 wherein the second modulation constellation comprises one of a PSK constellation and a QAM constellation.

5. (Original) The method of claim 1 wherein the signal processing operation comprises at least one of a finite impulse response (FIR) filtering operation, a Least-Mean-Squares (LMS) estimation operation, and a Maximum-Likelihood (ML) sequence detection operation using a Viterbi algorithm.

6. (Canceled)

7. (Canceled)

8. (Amended) The method of claim 1 wherein the selector comprises first and second switches and first and second add/subtract units, the first and second switches each selecting one of the real or the imaginary part of the element of the channel estimate for application to a corresponding one of the add/subtract units, such that the add/subtract units compute elements of real and imaginary parts of an inner vector product.

9. (Original) The method of claim 8 wherein an FIR filter operation is implemented using the selector by including feedback from outputs of the add/subtract units to corresponding inputs of the add/subtract units.

10. (Original) The method of claim 1 wherein the signal processing operation comprises a multi-stage multiplication operation implemented without multiplication operations, wherein each

stage of the multi-stage operation corresponds to a selector, and a left shift element is arranged between an output of a given one of the stages and a corresponding input of a subsequent stage.

11. (Original) The method of claim 1 wherein the signal processing operation is implemented utilizing a multi-stage hierarchical adder tree without multiplication operations.

12. (Amended) An apparatus for use in processing information in a receiver of a digital communication system, the apparatus comprising:

a signal processing circuit for processing a sequence of transmitted symbols, wherein the transmitted symbols correspond to points in a first modulation constellation, the first modulation constellation corresponds to a rotated version of a second modulation constellation, and each of the transmitted symbols represents a particular number of information bits;

wherein the signal processing circuit comprises at least one selector configured to compute a product of a channel estimate and a given one of the transmitted symbols; and

wherein the selector receives as inputs real and imaginary parts of an element of the channel estimate, and generates as outputs real and imaginary parts of a product of the element of the channel estimate and a corresponding element of the given symbol, without requiring a multiplication operation.

13. (Original) The apparatus of claim 12 wherein use of the first modulation constellation allows the signal processing operation to be performed without multiplication operations.

14. (Original) The apparatus of claim 12 wherein the first modulation constellation is generated by applying a 45° rotation to the second modulation constellation.

15. (Original) The apparatus of claim 12 wherein the other modulation constellation comprises one of a PSK constellation and a QAM constellation.

16. (Original) The apparatus of claim 12 wherein the signal processing circuit comprises at least one of a finite impulse response (FIR) filter, a Least-Mean-Squares (LMS) estimator, and a Maximum-Likelihood (ML) sequence detector implemented using a Viterbi algorithm.

17. (Canceled)

18. (Canceled)

19. (Amended) The apparatus of claim 12 wherein the selector comprises first and second switches and first and second add/subtract units, the first and second switches each selecting one of the real or the imaginary part of the element of the channel estimate for application to a corresponding one of the add/subtract units, such that the add/subtract units compute elements of real and imaginary parts of an inner vector product.

20. (Original) The apparatus of claim 19 wherein the signal processing circuit comprises an FIR filter implemented using the selector configured with feedback from outputs of the add/subtract units to corresponding inputs of the add/subtract units.

21. (Original) The apparatus of claim 12 wherein the signal processing circuit comprises a multi-stage circuit implemented without multiplication operations, wherein each stage of the multi-stage circuit corresponds to a selector, and a left shift element is arranged between an output of a given one of the stages and a corresponding input of a subsequent stage.

22. (Original) The apparatus of claim 12 wherein the signal processing circuit is implemented utilizing a multi-stage hierarchical adder tree without multiplication operations.

23. (Canceled)

24. (Amended) A method of processing information in a transmitter of a digital communication system, the method comprising the step of:

generating a sequence of transmitted symbols, wherein the transmitted symbols correspond to points in a first modulation constellation generated by applying a predetermined rotation to a second modulation constellation, and each of the transmitted symbols represents a particular number of information bits;

the transmitted symbols being configured such that a signal processing operation applied in a corresponding receiver of the system is implementable utilizing at least one selector configured to compute a product of a channel estimate and a given one of the transmitted symbols;

wherein the selector receives as inputs real and imaginary parts of an element of the channel estimate, and generates as outputs real and imaginary parts of a product of the element of the channel estimate and a corresponding element of the given symbol, without requiring a multiplication operation.

25. (Canceled)